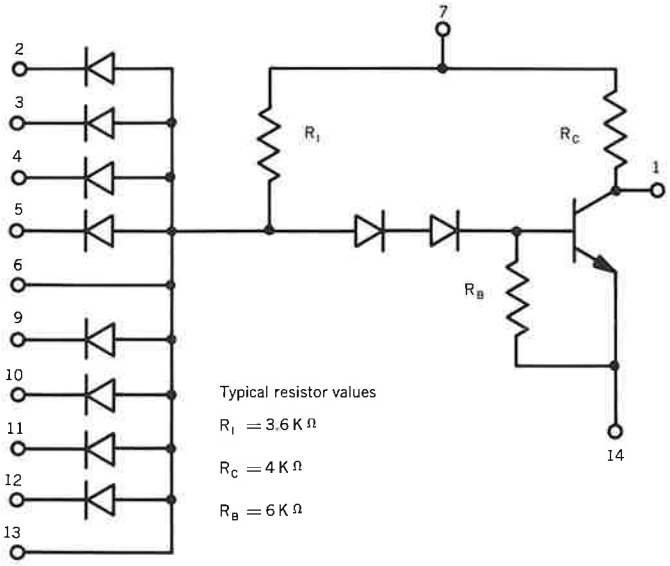
Equivalent circuit

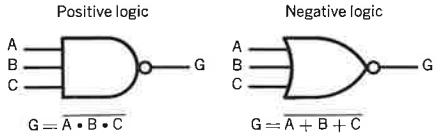


General description

The Westinghouse WM 234G single DTL NAND gate package includes a collector resistor and provides a fan-in capability of up to eight. In addition, two common anode points, termed the nodes, are available at external connections. These nodes permit added fan-in with use of diode expander arrays WM 217G or WM 227G. Also, the collectors of two or more NAND gates may be connected to form an AND-OR-NOT function as shown in Figure 14.

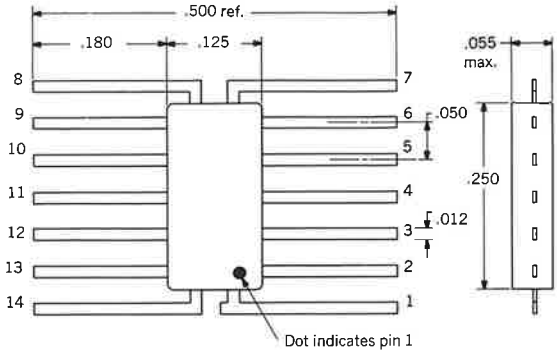
NAND/NOR function

This gate accomplishes the NAND logic function when the positive logic definition is used. When negative logic is used, the gate accomplishes the NOR logic function. Positive logic results when the more positive of the two voltage levels is defined as the 1-state.



Package

G style FLAT-PAK 0.1 grams



Design features †

- Fan-out 11 minimum
- One-state noise margin 3.80 v minimum
- Zero state noise margin 550 mv minimum
- Switching time 40 ns maximum
- Power consumption 15 mw maximum per gate

Reliability assurance

EVERY unit receives

- High temperature storage bake at +150°C
- 3 cycles of thermal shock −65°C to +100°C
- 30,000 G centrifuge
- Gross and helium hermeticitiy tests

† At V_{cc} = 6.0 v and at 25°C

WM 234G | **single DTL NAND gate**

technical data 91-210

Absolute maximum ratings①

Parameter	Symbol	Value	Units
Supply voltage	V_{cc}	+10	volts
Input voltage	V_{in}	+10②	volts
Node voltage	V_n	+1.2, −7	volts
Output voltage	V_{out}	+7②	volts
Ambient storage temperature	T_{stg}	− 65 to +175	°C
Ambient operating temperature	T_{opg}	−55 to +125	°C

Parameter	Symbol	Limit	Values at temperature −55°C	Values at temperature +25°C	Values at temperature +125°C	Units
Static electrical characteristics for $V_{cc} = +6.0$ volts						
Total power consumption						
Outputs ZERO-state	P_c, 0	max	19	20	18	mw
Outputs ONE-state	P_c, 1	max	13	11	9	mw
50% duty cycle	P_c	max	16	15	13	mw
	P_c	typ	11	11	9	mw
Input current, input grounded	I_n	max	2.10	1.80	1.50	ma
	I_n	min		1.00		ma
Node current, node grounded	I_{node}	max		2.1		ma
	I_{node}	min		1.1		ma
Input logic levels						
ZERO-state	V_{min}, 0	min	2.30	2.00	1.70	volts
ONE-state	V_{max}, 1	max	1.40	1.00	0.60	volts
Input diode reverse current	I_r	max		10.0	25.0	μa
with $V_{in} = 10$ v, $V_{oin} = 0$ v		typ		0.01	1.0	μa
Output current with $V_{in} = V_{min}$, 1	I_{out}	min	13.0	20.0	9.0	ma
at specified $V_{CE}(sat)$	$V_{CE}(sat)$		.55	.45	.35	volts
Output short circuit current	I_{sc}	max	2.10	1.90	1.50	ma
with $V_{in} = 0$ volts		min	1.15	1.0	0.8	ma
Output voltage with $I_{out} = 0$ and $V_{in} = V_{max}$, 0	V_{out}	min	5.90	5.80	5.40	volts
Fan-out available each gate	F_o	typ	9	16	10	
for $V_{cc} = 6.0$ volts ±5%	F_o	min	6	11	6	
ZERO-state noise margin③	$\triangle V_n$, 0	min	0.85	0.55	0.25	volts
ONE-state noise margin③	$\triangle V_n$, 1	min	3.60	3.80	3.70	volts
Dynamic electrical characteristics for $V_{cc} = +6.0$ volts						
Switching time (see Figures 1 and 2)						
Turn-on time	T_{on}	typ	22	20	18	ns
Turn-off time	T_{off}	typ	35	44	59	ns
Average switching time	T_{avs}	typ	28	32	38	ns
$(T_{on} + T_{off}) \div 2$	T_{avs}	max		40		ns
Ring propagation delay time (see Figure 11, ring of 15 gates, $C_o = 10$ pf)	T_{rpd}	typ	18	19	23	ns

① Limiting values beyond which the serviceability of the device may be impaired.
② These terminals must not be biased negatively with respect to ground.
③ Minimum ONE-state noise margin is given by (V_{out}, min—V_{min}, 1) where V_{out} is the minimum ONE-state output, and V_{min},1 is the minimum ONE-state input for ZERO-state output. Minimum ZERO-state noise margin is given by V_{max}, 0 — $V_{CE}(sat)$ where V_{max} is the maximum input voltage for a ONE-state output and $V_{CE}(sat)$ is the maximum output voltage in the ZERO-state at rated fan-out (6 or 11).

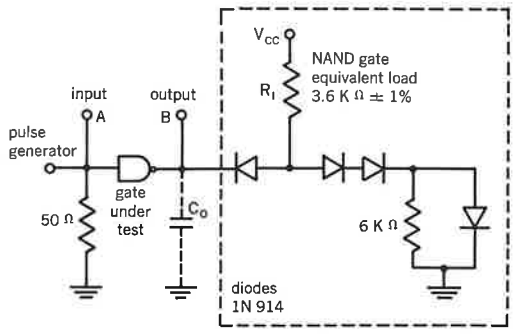


Figure 1 Total capacitance C_o is 10 pf which includes test jig and scope probe. Unused inputs are open circuited.

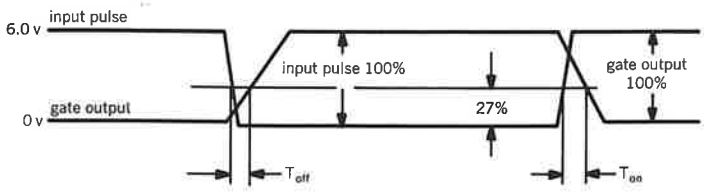


Figure 2 Average switching time: $T_{avs} = \frac{T_{on} + T_{off}}{2}$

Input pulse is 15 ns rise and fall, 200 ns width, 6 volt amplitude, and 100 kc repetition rate.

Typical electrical characteristics

Output and input current versus temperature and supply voltage

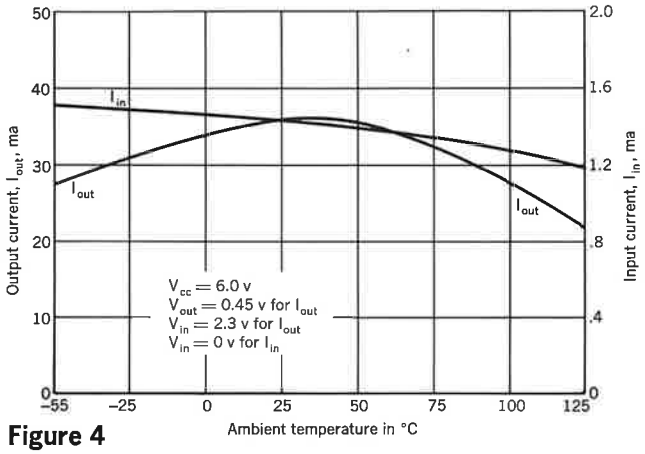


Figure 4

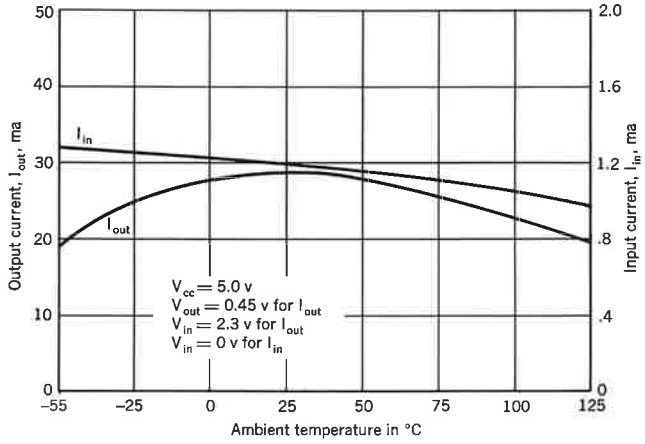

Output current, I_{out}, ma
Input current, I_{in}, ma
Ambient temperature in °C
I_{in}
I_{out}
$V_{cc} = 5.0$ v
$V_{out} = 0.45$ v for I_{out}
$V_{in} = 2.3$ v for I_{out}
$V_{in} = 0$ v for I_{in}

Figure 5

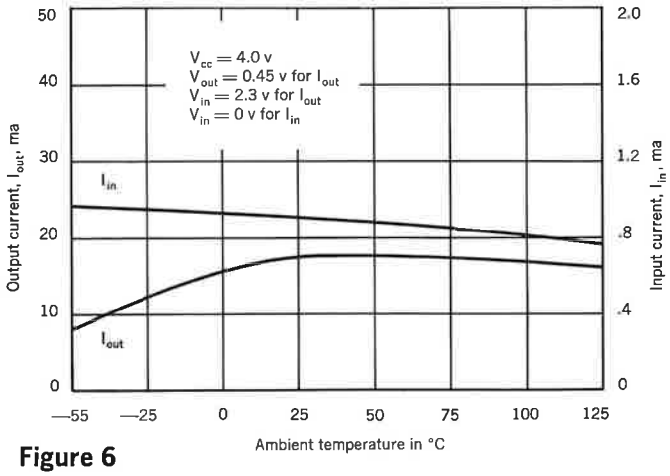

Output current, I_{out}, ma
Input current, I_{in}, ma
Ambient temperature in °C
I_{in}
I_{out}
$V_{cc} = 4.0$ v
$V_{out} = 0.45$ v for I_{out}
$V_{in} = 2.3$ v for I_{out}
$V_{in} = 0$ v for I_{in}

Figure 6

Output saturation characteristic versus temperature

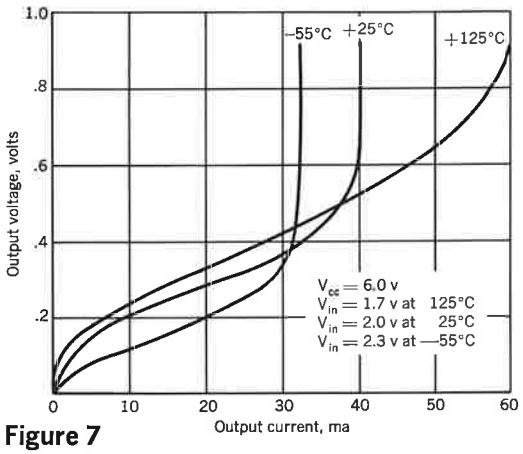


Figure 7

Output voltage versus input voltage and temperature

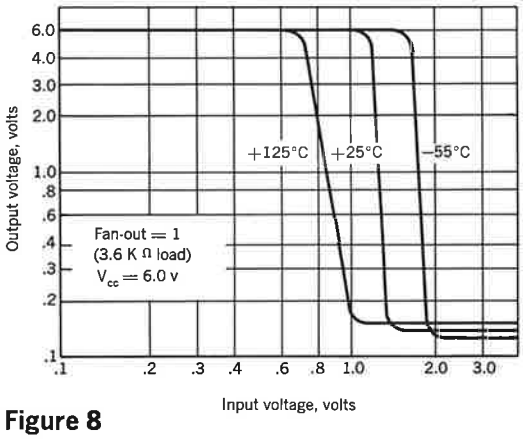


Figure 8

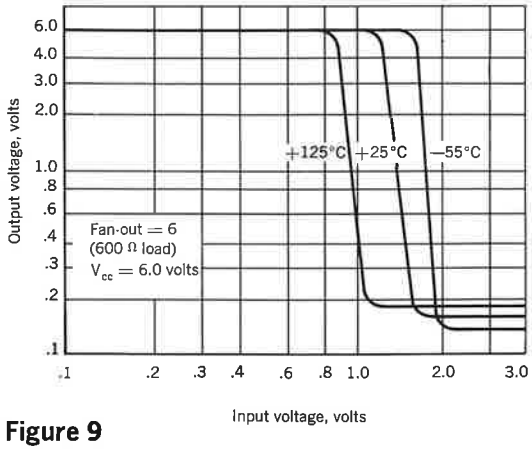


Figure 9

Typical electrical characteristics

Power consumption (50% duty cycle)

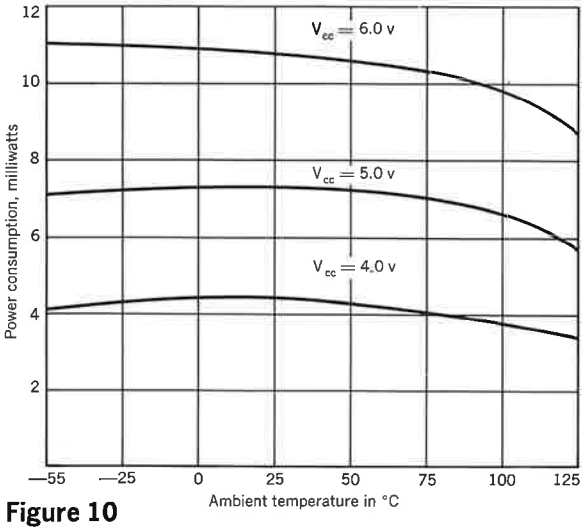


Figure 10

Fan-out test circuit (all gates)

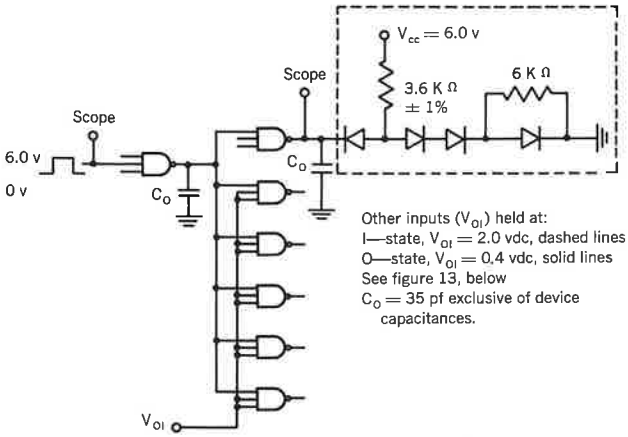


Figure 12

Ring propagation delay time versus supply voltage and temperature

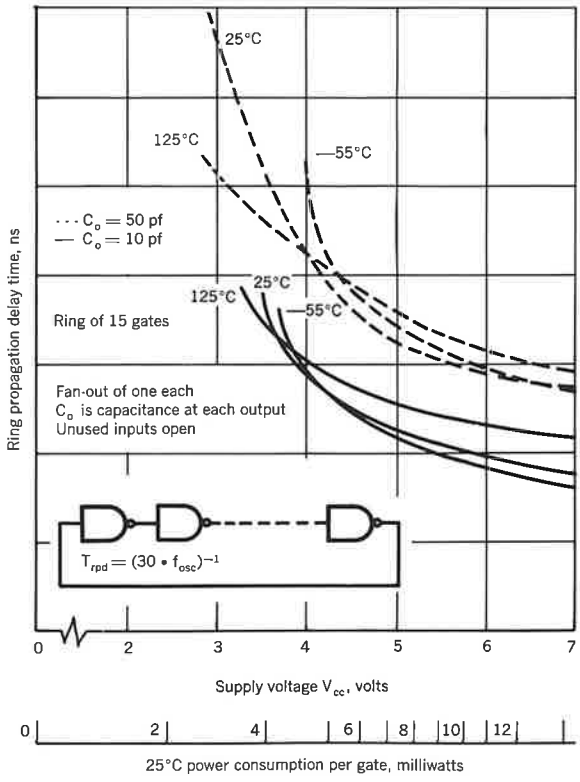


Figure 11

Propagation time versus fan-out

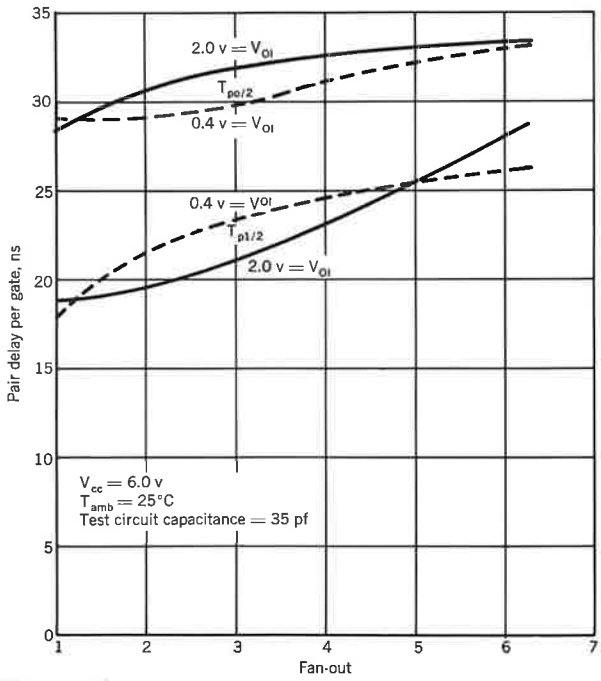


Figure 13

AND-OR-NOT function

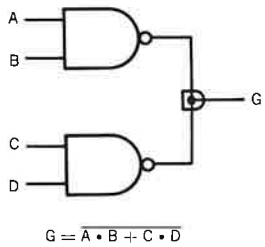


Figure 14

The AND-OR-NOT function is obtained by connecting together the terminals of two or more gates, as illustrated in Figure 14. In this configuration, two levels of logic are accomplished in one gate switching time.

For complete listings of compatible Westinghouse DTL integrated circuits consult Quick Reference Guide 91-000. For price information, consult OEM price list 91-120. All product specifications are subject to design change for product improvement.

Fan-out available versus number of additional gates paralleled

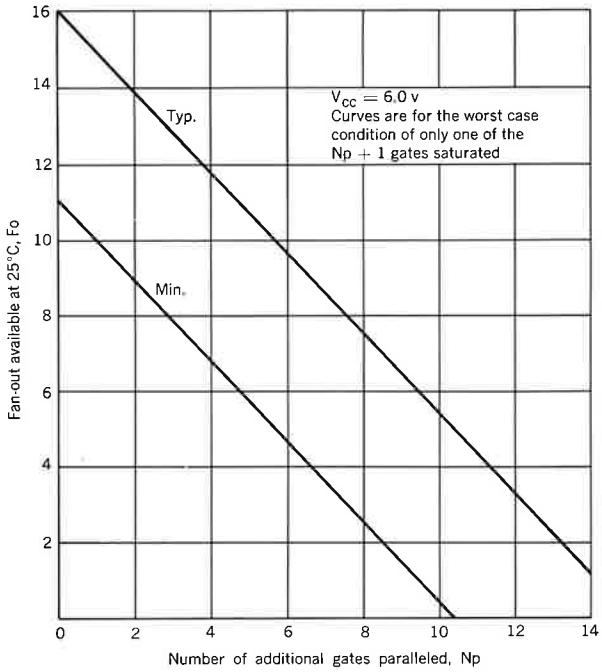


Figure 15

View showing the extensive cleanroom facilities in continuous operation for the manufacture of Westinghouse Integrated Circuits.

Westinghouse Electric Corporation / *MOLECULAR ELECTRONICS DIVISION*

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